

INFORMATION DISCLOSURE STATEMENT
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 Serial Number
 To Be Assigned

 Applicant(s)
 Park et al.

 Filing Date
 August 26, 2003

 Group Art Unit
 To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE (IF APPROPRIATE)
TT	A	5,274,588	12/28/93	Manzur, et al.			
TT	B	5,494,838	02/27/96	Chang, et al.			
TT	C	5,508,955	04/16/96	Zimmer, et al.			
TT	D	6,013,552	01/11/00	Oyama			
TT	E	5,856,223	01/05/99	Wang			
TT	F	6,281,545	08/28/01	Liang, et al.			
TT	G	6,329,248	12/11/01	Yang			
TT	H	6,365,449	04/02/02	Kuo, et al.			
TT	I	6,538,276	03/25/03	Hsieh, et al.			

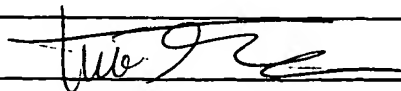
FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	NO

OTHER DOCUMENTS

TT	J	U.S. Patent Application Serial Number 10/358,645 entitled "VIRTUAL GROUND SINGLE TRANSISTOR MEMORY CELL, MEMORY ARRAY INCORPORATING SAME AND METHOD OF OPERATION THEREOF", filed February 4, 2003.						
TT	K	Yamauchi, Yoshimitsu, et al., "A New Cell Structure for Sub-quarter Micron High Density Flash Memory", 1995 International Electron Devices Meeting TECHNICAL DIGEST, IEEE, pp. 267-270, December 10-13, 1995.						

Examiner:



Date Considered:

01/05